



neo
semiconductor

X-DRAM™

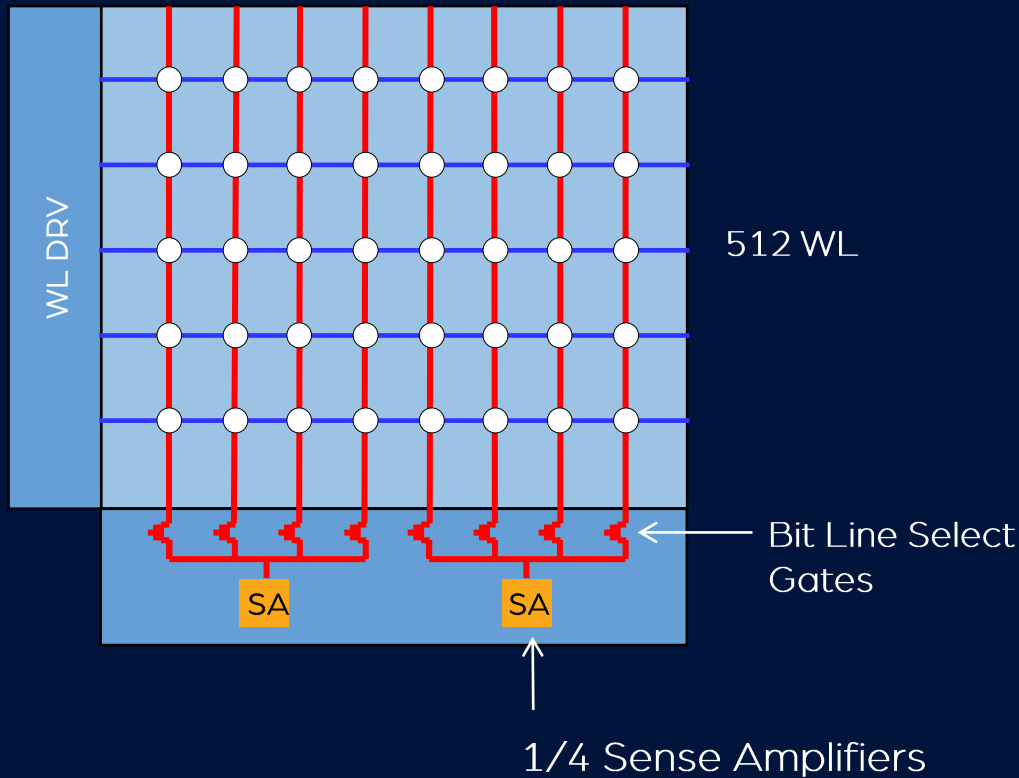
World's Lowest Power Consumption DRAM

August 2023

© 2023 Neo Semiconductor
Presentation | X-DRAM Technology



World's Lowest DRAM Power Consumption



15%

Refresh Power Consumption

25%

Bit Line Power Consumption

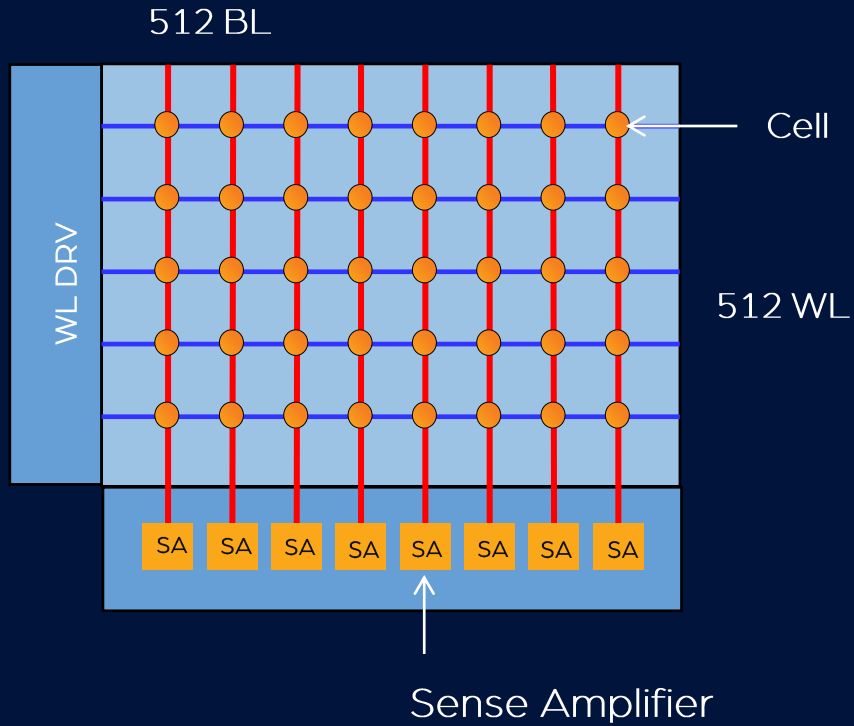
0%

Cost Increase

DRAM vs. X-DRAM

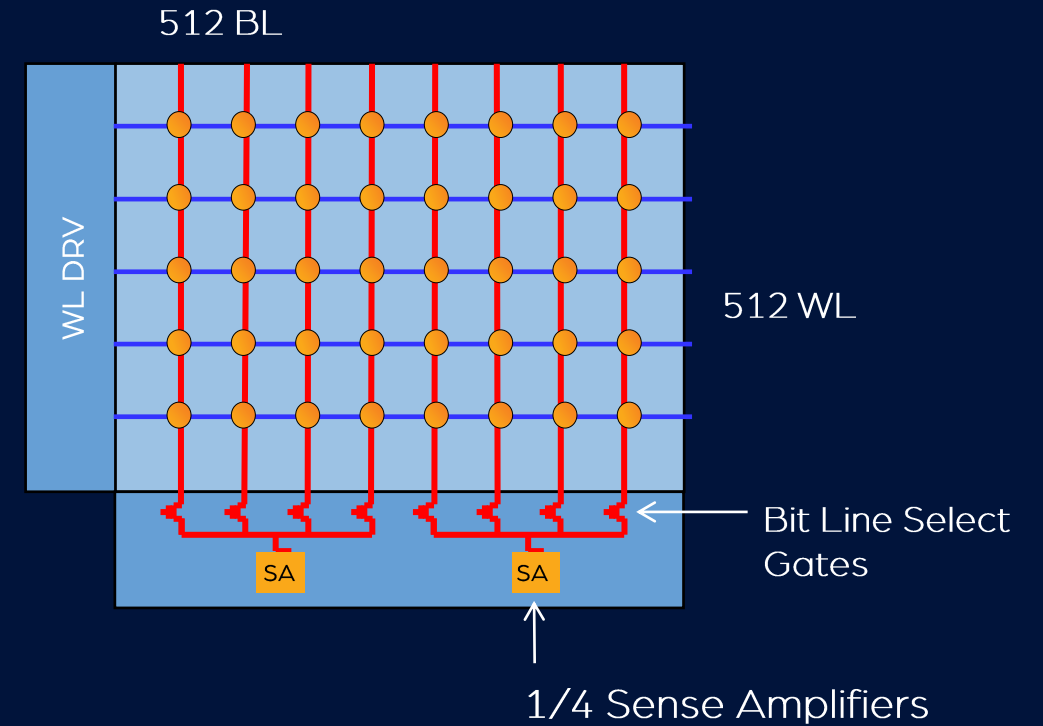
Conventional DRAM

Dedicated Sense Amplifiers



X-DRAM

Shared Sense Amplifiers



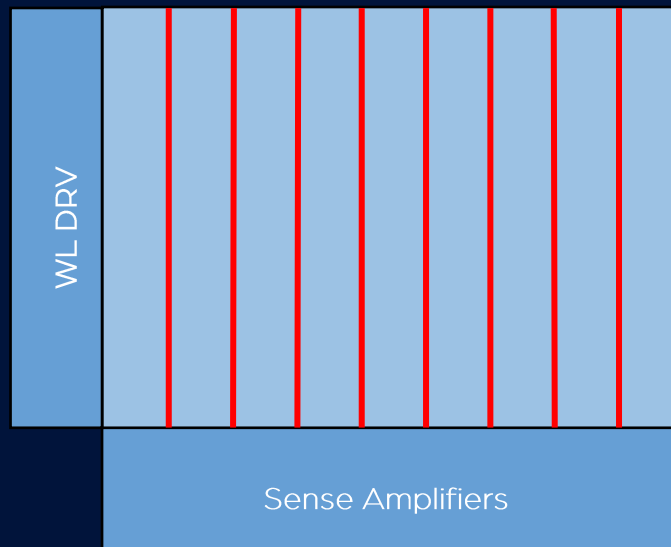
**Shared Sense Amplifiers
reduces layout size to 25%**

DRAM vs. X-DRAM

Architecture

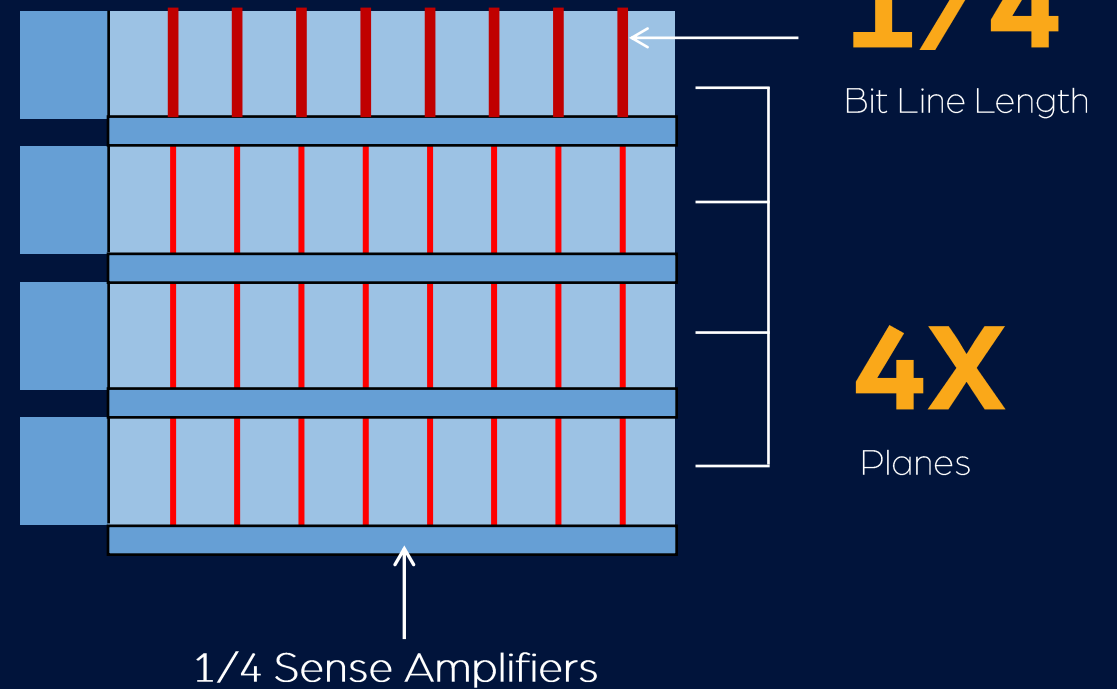
Conventional DRAM

Dedicated Sense Amplifiers



X-DRAM

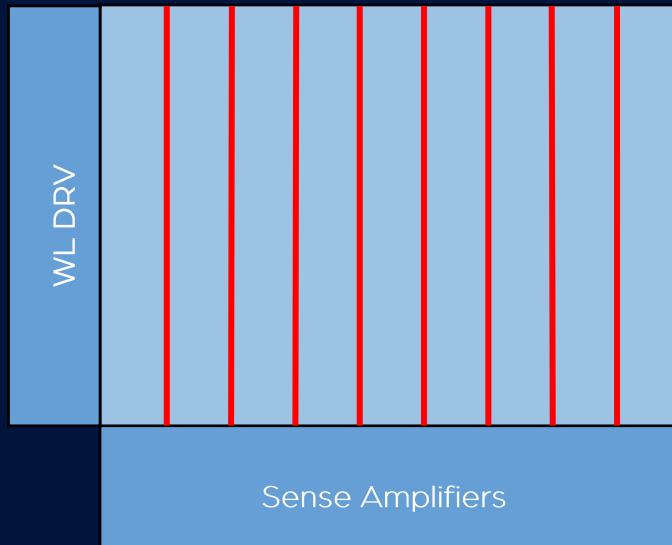
Shared Sense Amplifiers



DRAM vs. X-DRAM

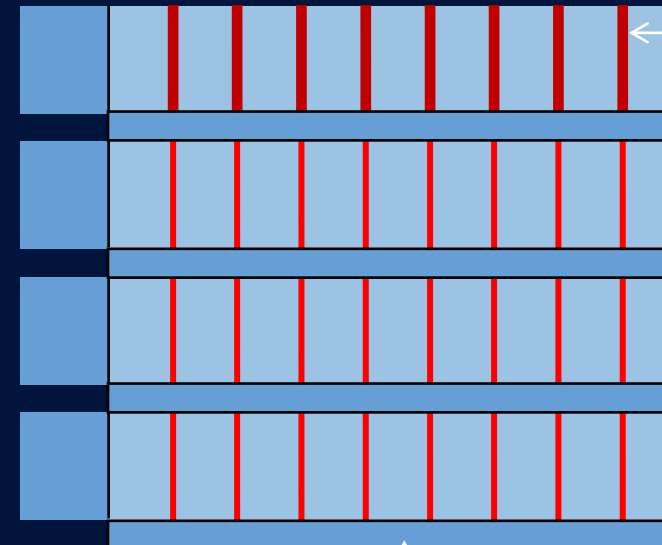
Conventional DRAM

Dedicated Sense Amplifiers



X-DRAM

Shared Sense Amplifiers



Same Die Size

25%

BL Delay

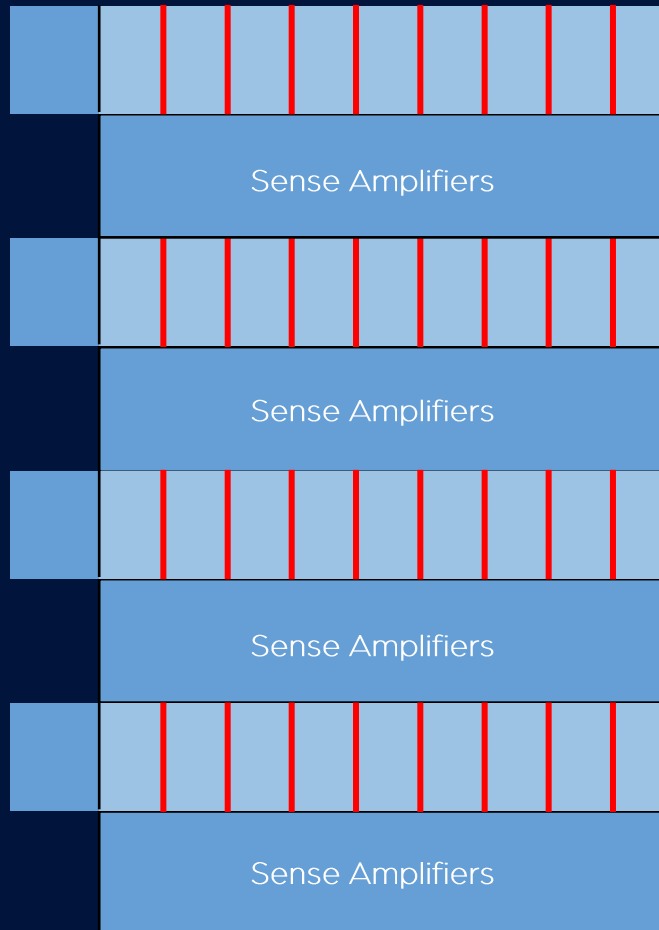
BL Power Consumption

Refresh Time

1/4 Sense Amplifiers

DRAM vs. X-DRAM

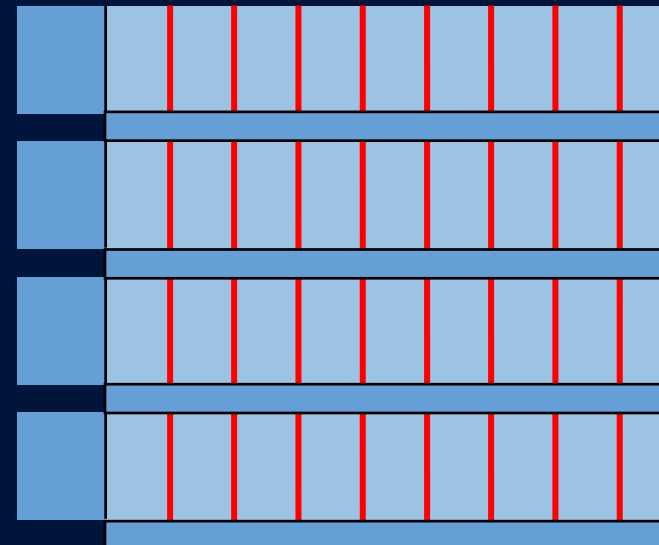
Conventional DRAM



4 planes

X-DRAM

- 4 planes: Increase die size to 160%
- 8 planes: Increase die size to 240%
- 16 planes: Increase die size to 300%



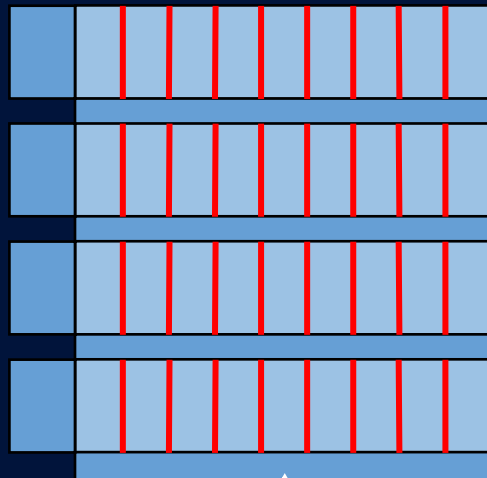
4 planes

X-DRAM

X-DRAM Architecture

X-DRAM

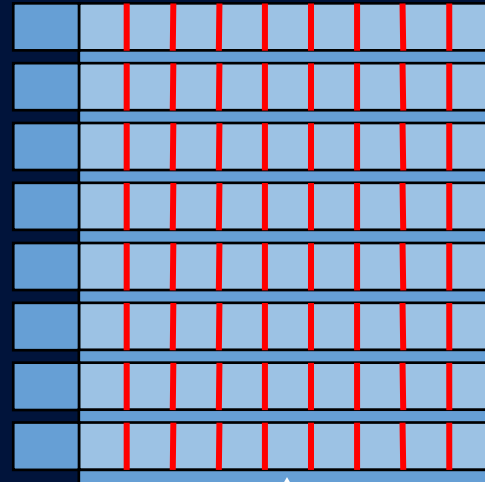
4X



1/4 BL

1/4 Sense Amplifiers

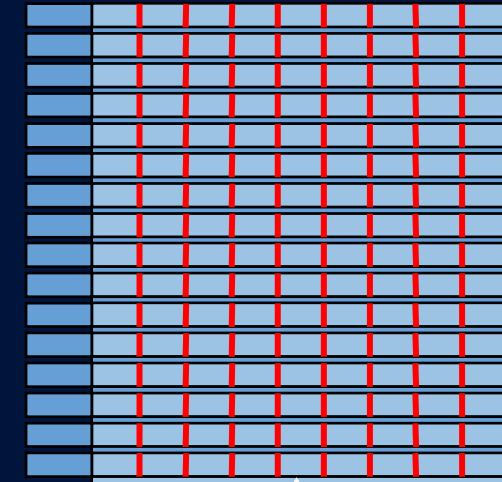
8X



1/8 BL

1/8 Sense Amplifiers

16X



1/16 BL

1/16 Sense Amplifiers

X-DRAM can be partitioned to various plane numbers without increasing die size.

X-DRAM Advantages (4X)

Advantage

FASTER
PERFORMANCE

50%

Activation
Latency

400%

Refresh Data
Throughput

25%

Refresh Time

LOWER
VOLTAGE

4X

BL Charge-Sharing
Voltage Margin

75%

Min. Cell Capacitor
Voltage

75%

Lower VDD Voltage

REDUCED
POWER

25%

BL Power
Consumption

50%

Refresh Frequency

15%

Refresh Power
Consumption

* Based on simulation



neo
semiconductor

Next Gen Memory Architectures

© 2023 NEO Semiconductor

www.neosemic.com

X-DRAM Tech 7C