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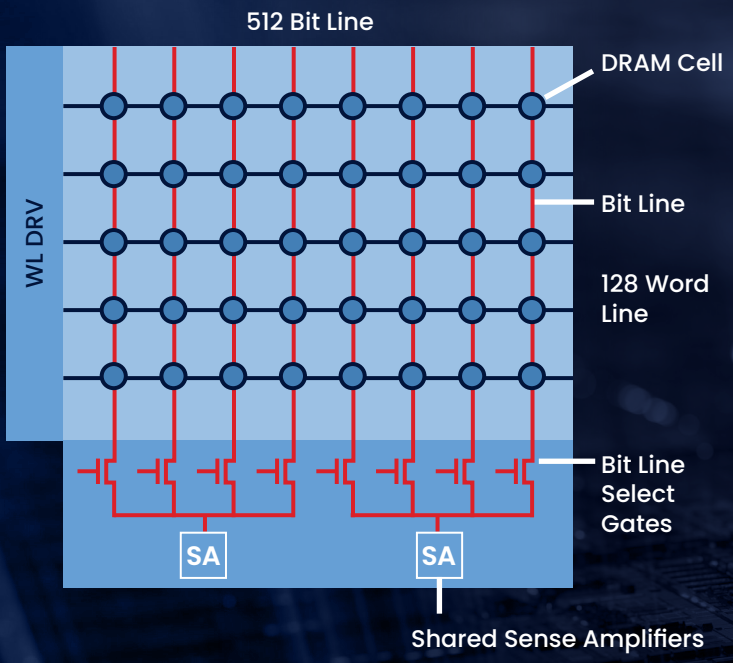
Next Gen Memory Architectures

X-DRAM™

Ultra High Speed, Ultra Low Power
Next Gen Architecture for DRAM



Bit lines and word lines connect to cells and are used to read and write data to the cells.

Sense amplifiers are used to read data stored at low power levels in the bit lines from cells.

Bit Line Select Gates switch Bit Lines to Sense Amplifiers.

Dynamic Random-Access Memory (DRAM) is used to support processors, making DRAM usage common in electronic devices. However, processor speeds have grown at higher rates than memory speeds across multiple generations, and the resulting "performance gap" widens annually. Power-sensitive environments like cloud data centers increasingly rely on higher-power processors and larger amounts of main memory to meet performance requirements.

Adopting X-DRAM architecture reduces power consumption, lowers latency, and increases throughput to overcome challenges that occur when using conventional DRAM. This results in:

- Higher performance for business systems (e.g., servers)
- Longer battery life for mobile devices (e.g., smartphones)
- More capabilities for edge computing devices (e.g., routers)
- New deployment options for Internet of Things objects (e.g., gateways)

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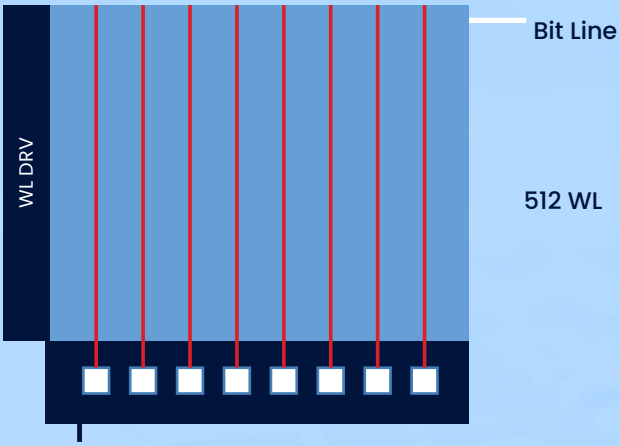
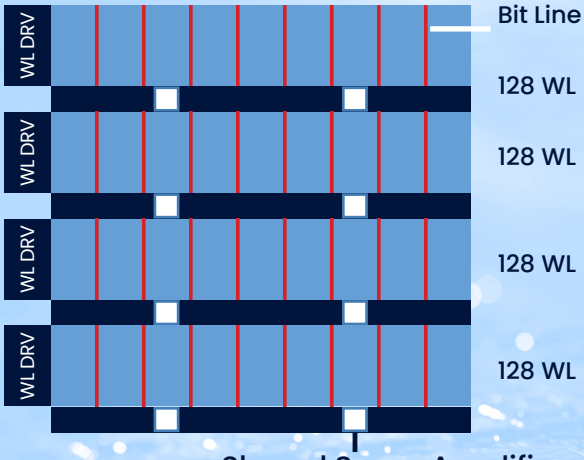
Conventional DRAM
Long Bit Line Length



X-DRAM
Short Bit Line Length



X-DRAM architecture reduces bit line length and capacitance to reduce the bit line delay and power consumption. Also, X-DRAM increases parallelism to increase data throughput and reduce refresh time and refresh power.

FASTER PERFORMANCE	**50%** Activation Latency	**400%** Refresh Data Throughput	**25%** Refresh Time
LOWER VOLTAGE	**4X** BL Charge-Sharing Voltage Margin	**75%** Min. Cell Capacitor Voltage	**65%** Lower VDD Voltage
REDUCED POWER	**25%** BL Power Consumption	**50%** Refresh Frequency	**15%** Refresh Power Consumption