New 1T1C and 3T0C Cells in the 3D X-DRAM Family: Advancing 3D NAND-like DRAM Technology Using IGZO

Fu-Chang Hsu, Richard J. Huang, Chia-Haur Chang, Re-Peng Tsay, Jui-Hsin Chang, I-Wei Huang

***Abstract*— 3D X-DRAM represents a groundbreaking advancement in 3D DRAM technology, leveraging a 3D NAND-like cell structure. This innovative design can be fabricated using a modified 3D NAND process, significantly reducing development costs and challenges. The original 3D X-DRAM is based on 1T0C Floating Body Cell technology. In this paper, we introduce two new types of 3D X-DRAM cells: the 1T1C and 3T0C cell structures. Compared to the original 1T0C design, the 1T1C design improves charge retention, while the 3T0C design enables current sensing. The newer designs incorporate IGZO channels, offering longer retention time and lower refresh power. Furthermore, they deliver incredibly high capacity and bandwidth to meet the demands of modern AI applications. Together, these three cells address the diverse technology roadmaps of various DRAM manufacturers, uniquely providing compatibility with existing processes and market requirements.**

INTRODUCTION

DRAM scaling has reached a critical bottleneck due to the challenges of shrinking capacitors below the 10 nm technology node. This has created a pressing need for monolithic 3D DRAM arrays, despite the significant complexities involved currently in developing a viable 3D process for DRAM. To address these challenges, we introduced an innovative cell structure known as 3D X-DRAM, the world's first 3D NAND-like DRAM built on Floating Body Cell (FBC) technology [1]. Featuring a donut-shaped cell structure, this design enables manufacturing using a modified 3D NAND process, allowing the stacking of hundreds of cell layers to achieve densities exceeding 128 Gb.

We have expanded the groundbreaking 3D X-DRAM technology into a comprehensive product family in response to specific commercial demands. Acknowledging that major DRAM manufacturers are pursuing 3D DRAM with traditional one-transistor, one-capacitor (1T1C) cell structures, we developed a 1T1C variant of 3D X-DRAM. This new design retains the 3D NAND-like architecture, ensuring compatibility with advanced manufacturing techniques while seamlessly aligning with existing DRAM roadmaps. FIG. 1 illustrates a fundamental 3D array structure based on the 3D X-DRAM cell design.

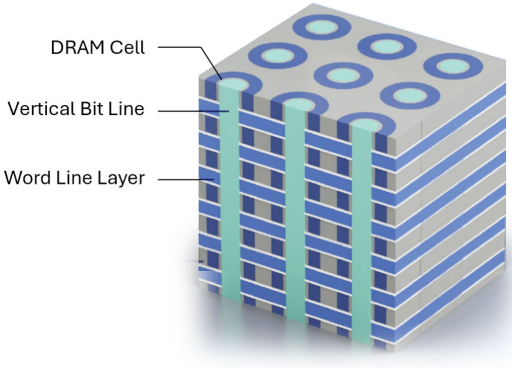

FIG. 1 - 3D X-DRAM array

The array consists of multiple word line (WL) layers and vertical bit lines (BL), with DRAM cells formed between the word line layers and connected to bit lines in parallel, enabling high-speed random access. The donut-shaped cell structure facilitates fabrication using a 3D NAND-like "punch and plug" process. This method allows simultaneous cell formation across all layers to optimize density and cost.

3D X-DRAM. 1T0C

FIG. 2 illustrates the original 3D X-DRAM, now referred to as 3D X-DRAM 1T0C (one transistor, zero capacitor) [1]. This cell employs a floating body to store electric holes representing data. The holes in the floating body modulate the threshold voltage of the cell and enable current-sensing during read operations, making it well-suited for both DRAM and in-memory computing (IMC). A proof-of-concept test chip is currently in progress.

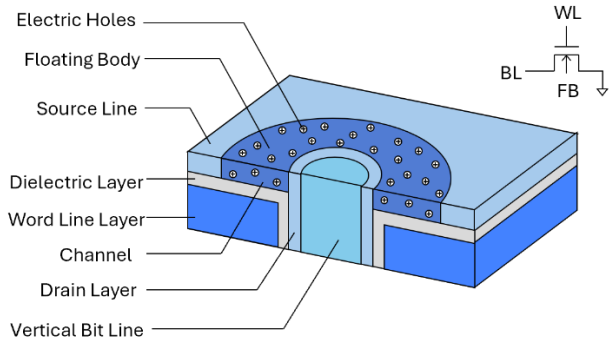

FIG. 2 - 3D X-DRAM. 1T0C cell structure

3D X-DRAM. 1T1C

The new 1T1C design is illustrated in FIG. 3. FIG. 4 removes the top word line layer to reveal the inner structure of the cell. This cell cleverly integrates one transistor and one capacitor into a compact cell structure. The transistor channel is composed of a thin oxide-based semiconductor layer, such as IGZO (Indium Gallium Zinc Oxide). IGZO is known for its extremely low off-current, which can enhance cell retention time. Alternatively, the cell can also use silicon or polysilicon as channel materials.

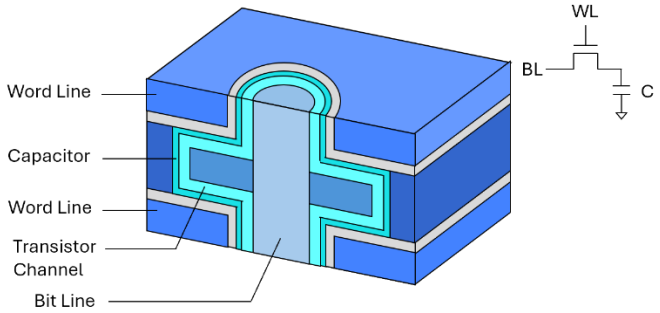

FIG. 3 - 3D X-DRAM. 1T1C cell structure

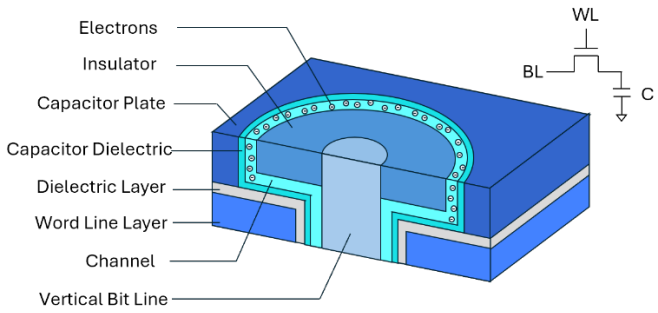

FIG. 4 - 3D X-DRAM. 1T1C cell structure

The IGZO layer is coupled to a metal word line layer, which acts as the transistor gate. The drain of the IGZO layer connects to a vertical bit line made of materials. A thin high-k dielectric layer, serving as a capacitor, is formed along the cylindrical sidewall on the source side of the transistor between the IGZO channel and a capacitor plate layer. The capacitor plate, composed of conductors such as N+ polysilicon, is biased at VDD to facilitate effective electron storage in the N-type IGZO layer.

The capacitor value is determined by the cell dimensions. For example, with a 60 nm bit line diameter, 45 nm channel length, 50 nm cell height, and a 5 nm HfO_2 dielectric layer, the capacitor value is approximately 0.7 fF. Assuming an IGZO off-current of $3x10^{-19}$ A/μm [5] and defining the data retention criterion as a 0.1V drop in the capacitor's voltage, this configuration achieves a long retention time over 450 seconds.

A key factor in 1T1C DRAM is the capacitor-to-parasitic bit-line capacitance ratio, which must exceed 10% to ensure sufficient 100mV sensing voltage during read operations. Simulations indicate this ratio surpasses 10% for up to 128-layer 3D arrays, ensuring reliable sensing voltage. For arrays beyond 128 layers, the capacitor value can be enhanced by employing taller capacitor walls, thinner dielectric layers, or higher-k materials.

FIG. 5 showcases another cell structure incorporating additional spacers between vertical bit lines and word line layers to reduce parasitic bit line capacitance. These spacers, which may be formed from low-k dielectrics like silicon dioxide (SiO_2), play a critical role in enabling scalability. Simulation results indicate that adding spacers with a thickness of 5 nm enables the stacking of more than 512 layers of cells

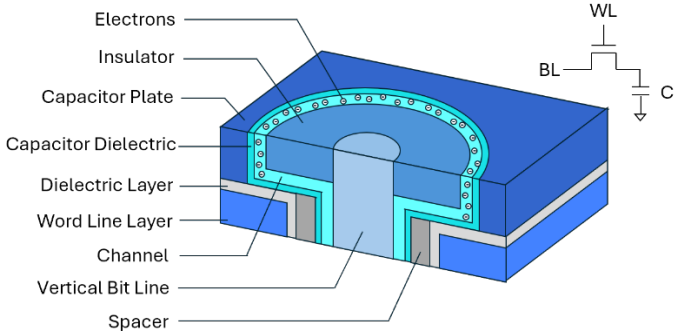

FIG. 5 - 3D X-DRAM. 1T1C cell structure with spacers

ALTERNATIVE 1T1C DESIGN

FIG. 6 illustrates a variation of the 1T1C design, where a conductor plate is connected to the source side of the IGZO channel, functioning as a capacitor electrode for electron storage. The capacitor structure consists of the conductor plate, the gate dielectric layer, and the word line layer, with its capacitance determined by the conductor plate's area.

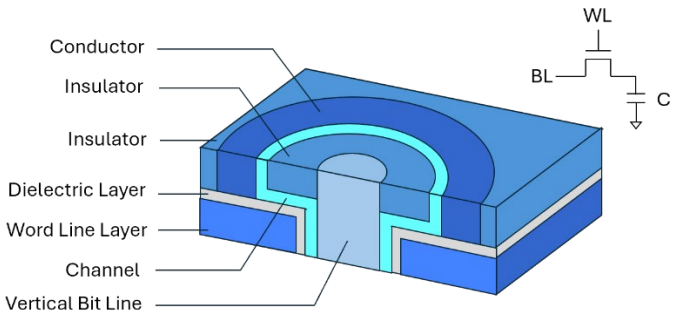

FIG. 6 - 3D X-DRAM. 1T1C cell variant

FIG. 7 presents another variation of the 1T1C design, similar to FIG. 6, but eliminating the insulator between the vertical bit line and the IGZO layer. This modification not only reduces the cell height but also enables the IGZO channel to be coupled by two word line layers, one above and one below, thereby enhancing channel control. Please note that, in addition to these variants, the 3D X-DRAM family includes many other proprietary cell structures. FIG. 6 and 7 illustrate only two examples.

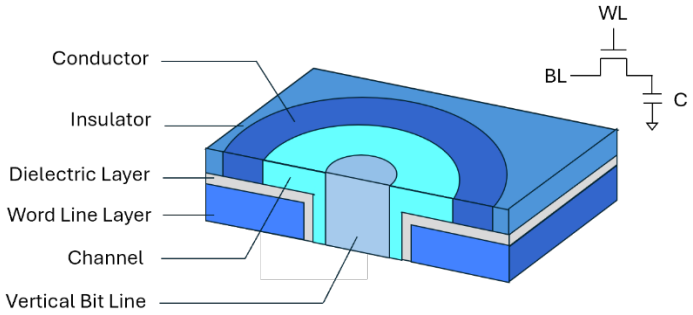

FIG. 7 - 3D X-DRAM. 1T1C cell variant

3D X-DRAM. 3T0C

FIG. 8 illustrates another variant of 3D X-DRAM cell technology, referred to as 3T0C (three transistors, zero capacitor). This innovative cell incorporates two IGZO layers for enhanced performance. The first IGZO layer is coupled to the word line layer to form the first channel. Its source connects to a metal gate. The word line can activate the first channel to store electrons in the metal gate.

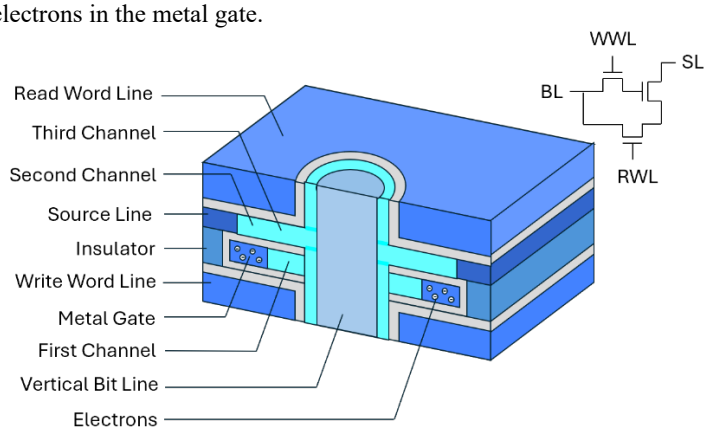

FIG. 8 - 3D X-DRAM. 3T0C cell structure

When the stored data is 1 (VDD), the metal gate activates the second channel formed by the second IGZO layer, allowing current to flow between the bit line and the source line. When the data is 0 (0V), the metal gate disables the second channel, preventing current flow. The read word line activates the third

channel, enabling the read operation. Since the 3T0C cell relies on current sensing, it is particularly well-suited for in-memory computing and artificial intelligence (AI) applications, where high-speed data processing and efficient power management are crucial.

CELL OPERATIONS

The operations of the 1T1C cell are demonstrated in FIG. 9: (a) shows the read/write condition. The selected word line is biased with VDD, activating the channel and allowing electrons to flow between the bit line and the capacitor. (b) shows the storage condition. The word line is set to a negative voltage (-V), deactivating the channel. The electrons stored in the capacitor are retained due to the VDD voltage applied to the capacitor plate. (c) shows the selection of the cell. In this configuration, even word lines (WL2, WL4) are connected to decoder circuits, while odd word lines are connected to a negative voltage (-V) to deactivate their respective channels. Since each even word line is shared between two adjacent cells, data is stored across both cells. This structure effectively doubles the capacitor storage size while eliminating the need for insulating layers between cells, simplifying the fabrication process.

Another benefit of this configuration is that the negative word lines effectively isolate cells in adjacent layers, solving word-line coupling, also known as the "row hammering" issue in DRAM, which can cause bit flips and data corruption.

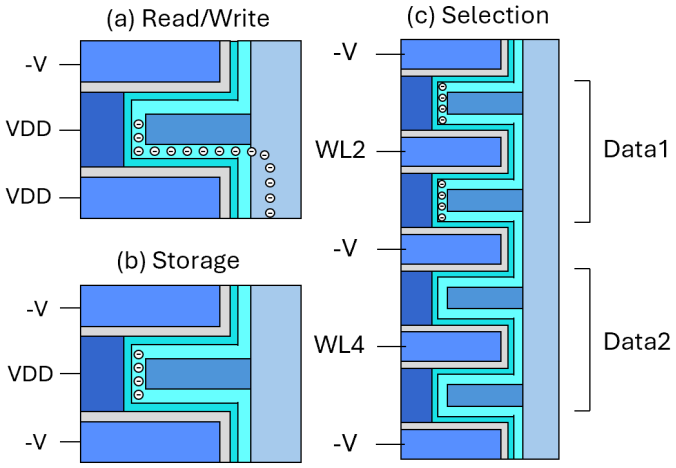

FIG. 9 - 3D X-DRAM. 1T1C operations

TCAD SIMULATIONS

FIG. 10 presents the results of TCAD (Technology Computer-Aided Design) simulations for the 1T1C cell.

- (1) and (2) illustrate electron concentration during write operations for data 1 and 0. The word line is set to 1.5V, activating the channel and enabling electron flow into the source-side capacitor. The capacitor plate is biased at 1.5V.
- (3) and (4) show the storage conditions for data 1 and 0. The word line is set to -1.5V, deactivating the channel and retaining the electrons within the source-side capacitor. Note that electrons accumulate for data 1 and deplete for data 0 at the interface of the polysilicon capacitor plate (node A), providing evidence that the capacitor stores 1V and 0V, respectively. Simulations show the write time is less than 8 ns.

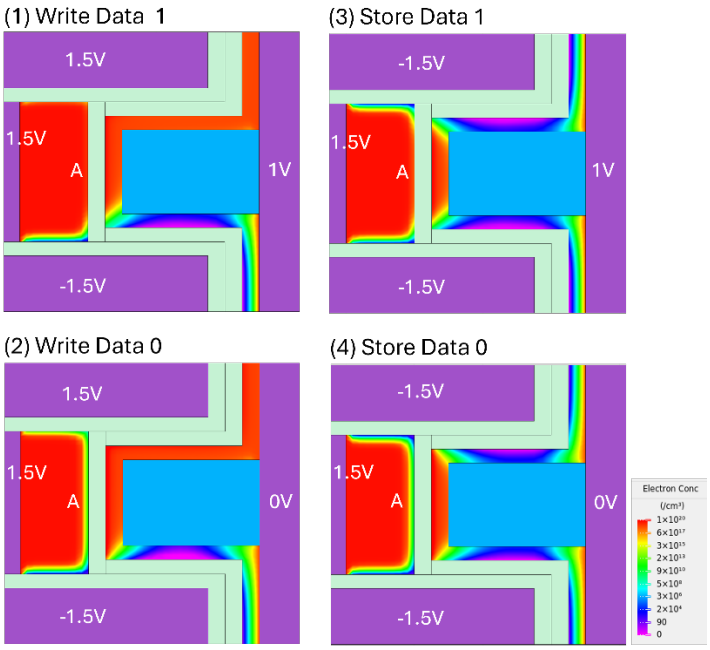

FIG. 10 – TCAD Simulations for the 1T1C cell

3D ARRAY ARCHITECTURE

The 3D array architecture of the 3D X-DRAM family is illustrated in FIG. 11. The array is segmented into multiple sectors by vertical slits. The multiple word line layers within each sector are connected to decoder circuits through staircase structures located along both edges of the array.

This 3D array architecture has been a proven industry standard for years, enabling the production of 3D NAND flash memory with over 300 layers. Building on this success, 3D X-DRAM innovatively adopts a similar array architecture with a smaller sector size. This design results in high-speed, high-density DRAM solutions tailored to advanced performance demands.

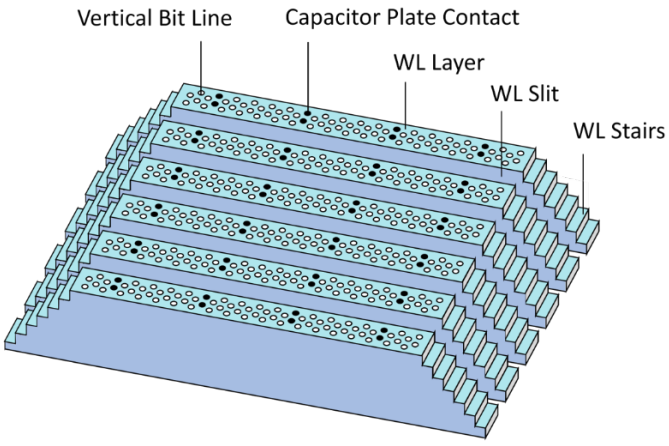

FIG. 11 - 3D array architecture of the 3D X-DRAM family

FABRICATION PROCESS

The 3D X-DRAM cell can be fabricated using a 3D NAND-like process, requiring only modifications to accommodate IGZO and capacitor formation. FIG. 12 highlights the key steps for manufacturing 1T1C cells:

1. Alternately deposit multiple conductive layers, like heavily doped polysilicon, and sacrificial layers.
2. Perform wet etching on the conductor layers to create recesses.
3. Sequentially deposit a dielectric layer followed by an IGZO layer. An oxygen annealing process may be applied to adjust IGZO's electrical properties.
4. Fill the recesses with an insulator.
5. Reform the vertical bit line holes and deposit metal to fill the bit line holes.
6. Remove the sacrificial layers, then deposit a dielectric layer on the sidewalls of the spaces. Subsequently, deposit metal to fill these spaces and form the word line layers, completing the 1T1C cell structure.

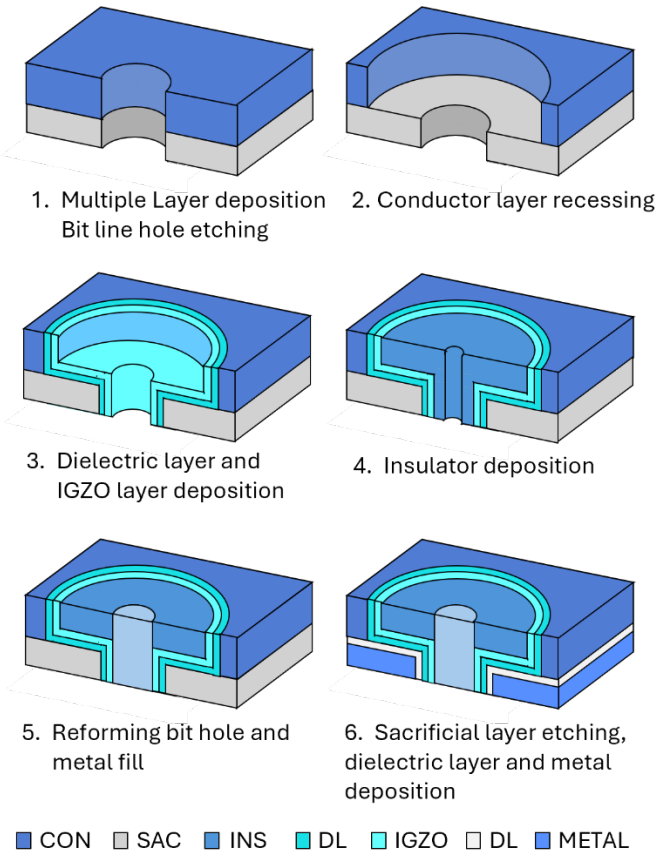

FIG. 12 - 3D X-DRAM. 1T1C cell fabrication process steps

This process offers several advantages:

1. It requires only a single mask for the bit line holes, ensuring that all process steps are fully self-aligned. This eliminates misalignment issues between masks, which is particularly critical for 3D arrays. As a result, the design significantly enhances process yield and enables stacking of more than 300 layers.
2. It simultaneously processes cells across all layers, unlike solutions that rely on a layer-by-layer approach. This significantly reduces manufacturing costs.
3. The process leverages well-established 3D NAND techniques, ensuring a faster development cycle and greater scalability.

BIT LINE SPACER PROCESS

FIG. 13 outlines additional process steps for forming the extra spacers in the cell structure depicted in FIG. 5:

1. After forming the vertical bit line holes, perform wet etching to recess the sacrificial layers.
2. Deposit an insulator to fill the recesses.
3. Remove the insulator from the sidewalls of the bit line holes. Leaving the remaining insulator in the recesses to form spacers. Then, follow process steps 2–6 in FIG. 12 to complete the cell structure shown in FIG. 5.

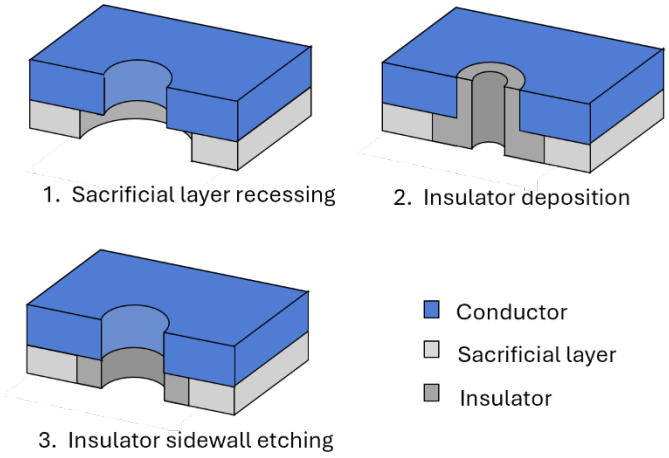

FIG. 13 - 3D X-DRAM spacer fabrication process steps

CAPACITOR RATIO

FIG. 14 shows the ratio between the cell capacitor and parasitic bit line capacitance as a function of the number of layers. Typically, this ratio needs to be higher than 10% to obtain a 100mV sensing voltage for a successful read operation.
For the 1T1C cell without spacers, the ratio is 25% for 64 layers and 12% for 128 layers, which is adequate for proper operation. However, the ratio can fall below 6% for 256 layers. For another 1T1C cell with spacers illustrated in FIG. 5, incorporating 5 nm spacers can effectively reduce parasitic bit line capacitance, thereby increasing the capacitor ratio to 19% for 256 layers and 10% for 512 layers. This improvement ensures sufficient sensing voltages up to 512 layers.

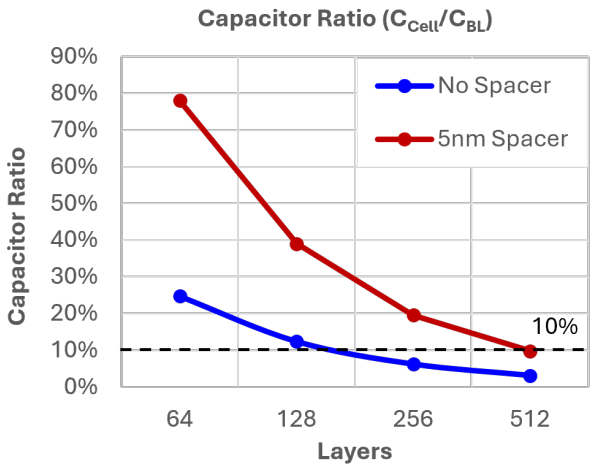

FIG. 14 - 3D X-DRAM.1T1C capacitor ratios

DATA RETENTION TIME

The data retention time of DRAM cells is influenced by both cell capacitor size and off-cell leakage current. FIG. 15 presents simulation results for the 3D X-DRAM 1T1C cell, showing retention time plotted against IGZO off-current, ranging from 10^{-18} to 10^{-20} A/μm [2]. The results indicate that cells with 50 nm and 70 nm heights achieve exceptionally long retention times—450 seconds and 750 seconds, respectively—under an IGZO off-current of 3×10^{-19} A/μm [5].

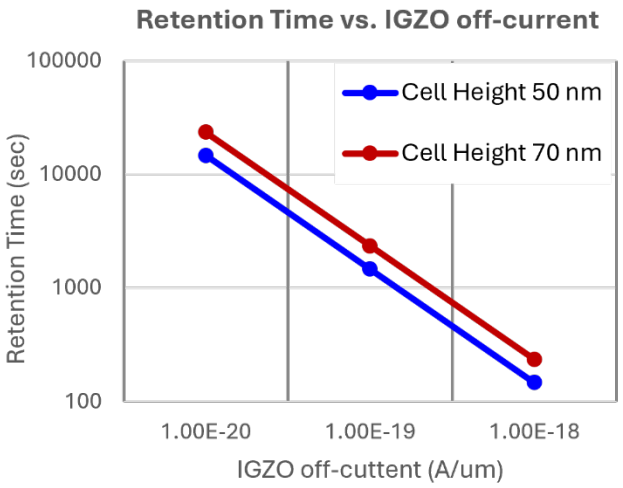

FIG. 15 - 3D X-DRAM 1T1C Retention Time

FIG. 16 illustrates the relationship between data retention time and cell capacitor size, ranging from 0.5 fF to 4 fF. With an IGZO off-current of 3×10^{-19} A/μm [5], the data retention time is approximately 550 seconds for a 0.5 fF capacitor and 4,400 seconds for a 4 fF capacitor. The simulation results show that a 0.5 fF capacitor is sufficient to achieve long data retention, thanks to IGZO's extremely low off-current.

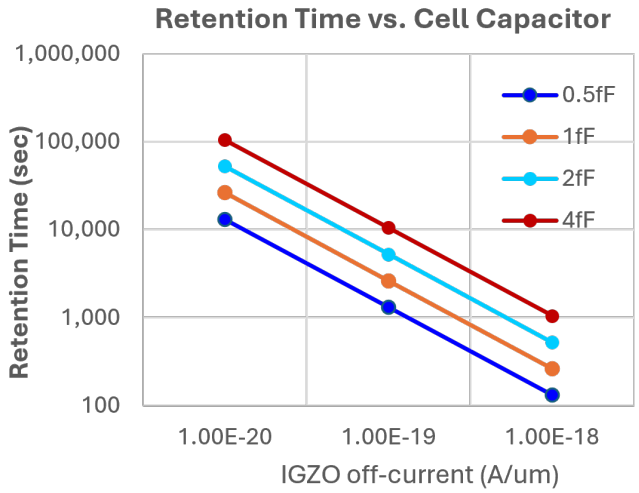

FIG. 16 – Retention time versus Cell Capacitor Size at different IGZO off-currents

CELL SIZE vs. CAPACITOR SIZE

FIG. 17 illustrates the relationship between cell size and cell capacitor size, based on the structures shown in FIG. 6 and 7. For reference, a predicted 2D DRAM cell size of 1,040 nm² at the 10 nm technology node [3] is used. Comparisons show that for a 128-layer array, the cell size with a 0.5 fF is 12%, and with 4 fF capacitor is 48% of that of a 10 nm 2D DRAM cell. In a 512-layer array, the cell size is further reduced to only 3% with a 0.5 fF capacitor, and 12% with a 4 fF capacitor.

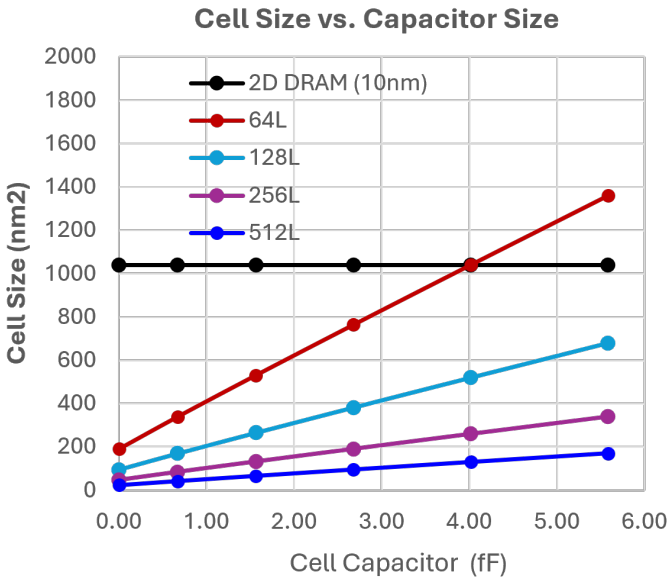

FIG. 17 – Cell Size versus Cell Capacitor Size

DENSITY COMPARISON

FIG. 18 presents a density comparison between the 3D X-DRAM 1T1C cell and conventional 2D DRAM. 3D X-DRAM increases the number of stacked layers to achieve higher density, whereas 2D DRAM reduces the cell size. According to public estimation, 2D DRAM at the 0a node can reach a density of 48Gb [3].

In contrast, 3D X-DRAM 1T1C cells can reach densities ranging from 64Gb to 512Gb, corresponding to 64 to 512 layers. This advancement overcomes the scaling limitations of 2D DRAM and continues to extend the density roadmap, positioning 3D X-DRAM as a competitive alternative for applications requiring higher density.

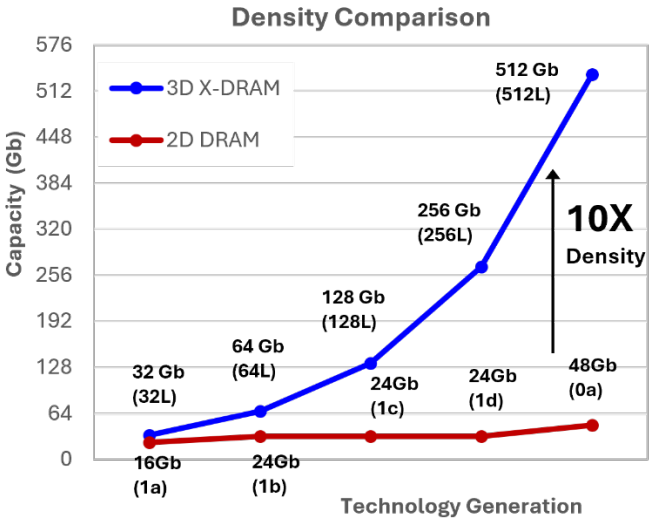

FIG. 18 – Density of 3D X-DRAM.1T1C versus 2D DRAM

BANDWIDTH COMPARISON

Beyond increasing density, 3D X-DRAM significantly enhances the bus width of high-bandwidth memory (HBM). FIG. 19 presents a bus-width comparison between the HBM utilizing 3D X-DRAM 1T1C and traditional HBM. Due to the limitations of through-silicon via (TSV) technology, the current HBM3E supports only a 1K bit bus width, while industry projects that HBM4 will expand this to 2K bits by 2026 [4].

In contrast, 3D X-DRAM's unique array structure eliminates the need for TSV and enables hybrid bonding technology, which can scale bus width beyond 4K bits to 32K bits, increasing bandwidth by up to 16X while significantly reducing power consumption and heat generation-- making it a game-changer for AI applications.

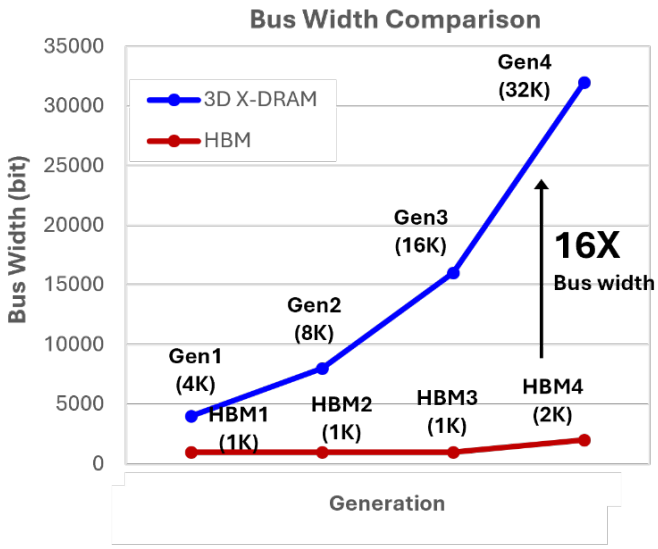

FIG. 19 – Bus width comparison of 3D X-DRAM vs. HBM

THE 3D X-DRAM FAMILY

The 3D X-DRAM technology has evolved into a family of three distinct cell types: 1T0C, 1T1C, and 3T0C. These cell designs are tailored to meet the requirements of diverse DRAM products and address varying market demands for different kinds of solutions. FIG. 20 provides a comparative overview of three 3D X-DRAM cells:

	3D X-DRAM Family		
	1T0C	**1T1C**	**3T0C**
Mechanism	Floating Body	Capacitor	Gain Cell
Channel	Polysilicon	IGZO	IGZO
Write	BTBT/Imp. Ion	Capacitor	Metal Gate Storage
Read	Current Sensing	Charge-sharing	Current Sensing
Retention	Medium	Long	Long
Destructive	No	Yes	No
Application	DRAM and IMC	DRAM	DRAM and IMC

FIG. 20 – Comparative overview of 3D X-DRAM cells

- 1T1C Cells: These are compatible with mainstream DRAM technology, enabling seamless integration into existing 3D DRAM roadmaps.
- 1T1C and 3T0C Cells: Both leverage IGZO channels, delivering significantly extended data retention times due to IGZO's exceptionally low off-cell current.
- 1T0C and 3T0C Cells: Featuring current-sensing mechanisms, these cells are ideal not only for DRAM applications but also for emerging in-memory computing and artificial intelligence (AI) applications.

PROOF OF CONCEPT

Proof-of-concept test chips for the 1T0C design are in progress, while those for the 1T1C design are currently in the planning stage, with availability expected in 2026.

CONCLUSION

With the introduction of 1T1C and 3T0C designs, the 3D X-DRAM family advances DRAM density and power efficiency while leveraging 3D NAND-like fabrication for scalable and cost-effective solutions. These novel designs enable 3D DRAM for modern and emerging applications, such as in-memory computing and artificial intelligence.

ACKNOWLEDGEMENT

The authors extend their sincere gratitude to Stan Shih, Max Wu, Jack Sun, Tuo-Hung Hou, Maya Lustig, Jay Kramer, Omar Barraza, Yao-Jen Lee, Yiming Li, Chang-Hong Shen, Chih-Chao Yang, Po-Jung Sung, and Derek Kimpton for their invaluable support.

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