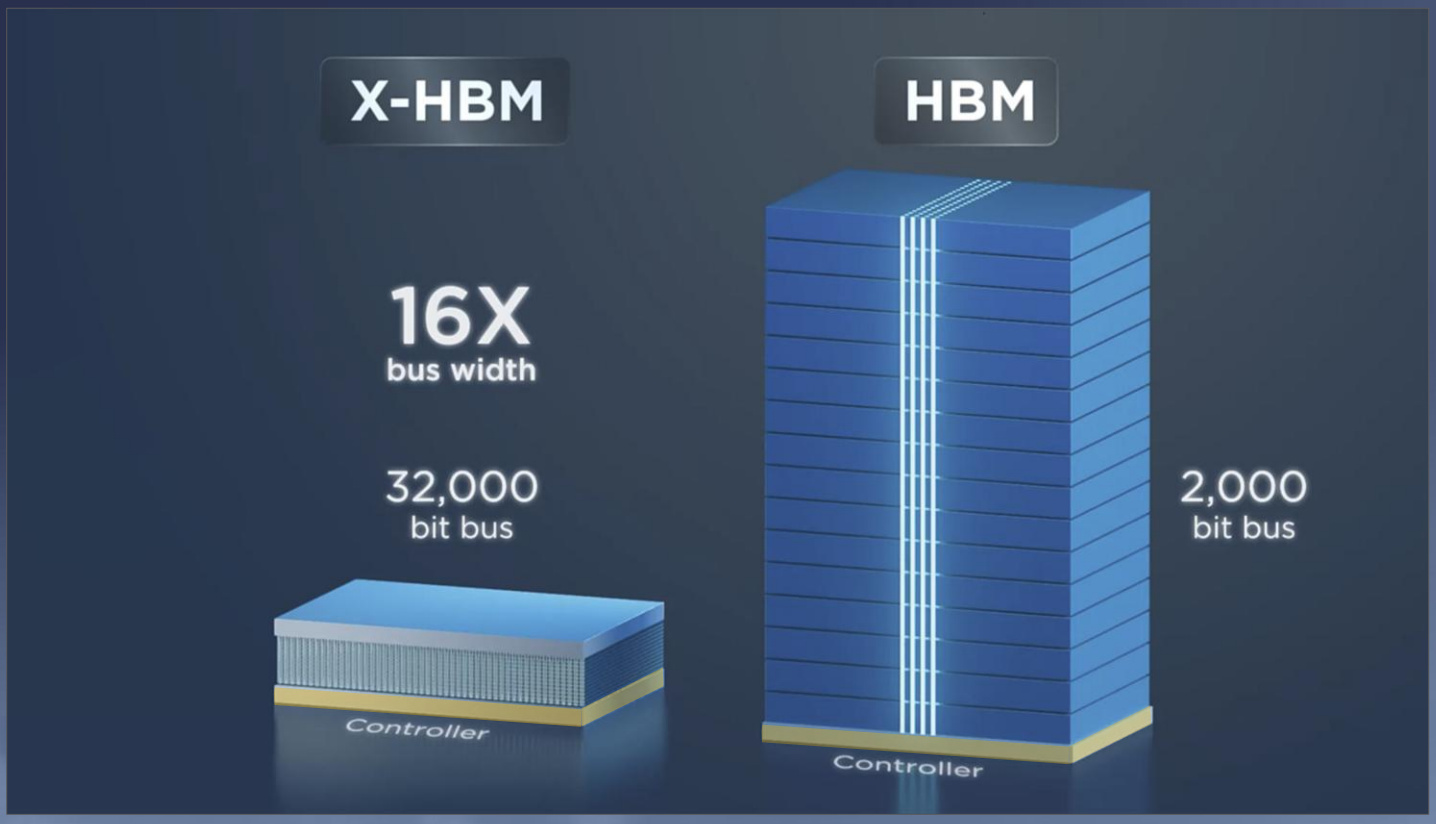
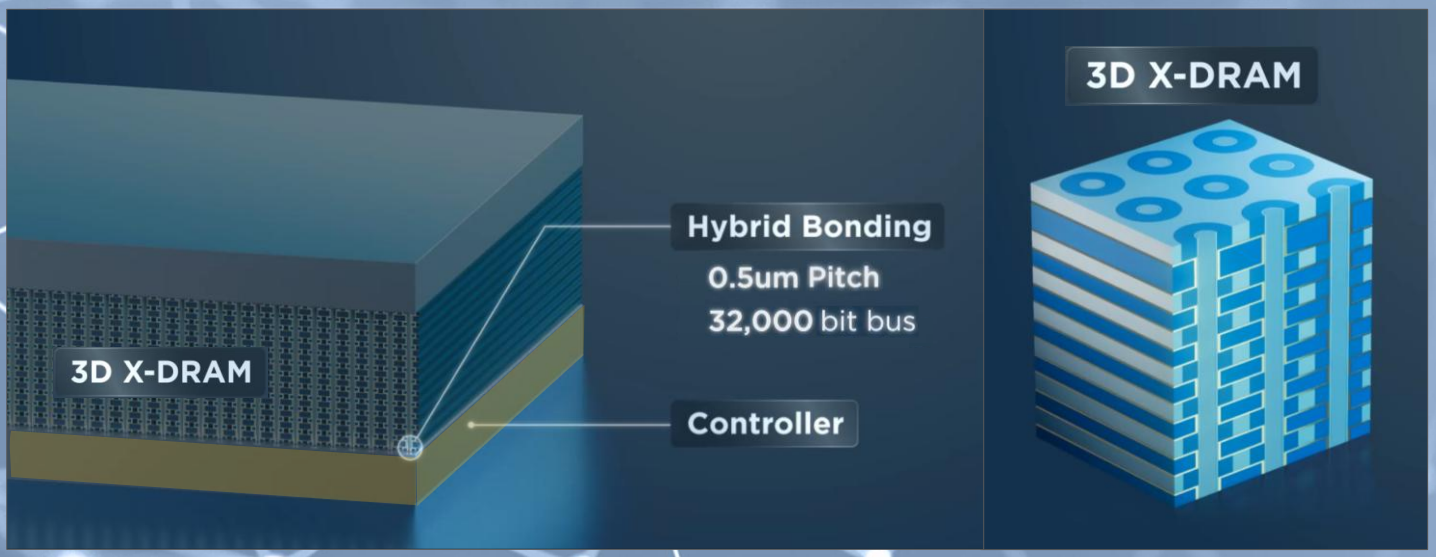
neo semiconductor

X-HBM™

Accelerate AI with 16X Higher Bandwidth



X-HBM is based on NEO Semiconductor's 3D X-DRAM technology, which forms a 3D array with hundreds of layers of DRAM cells on the surface of a single die. With today's technology, the array can reach up to 300 layers, providing 300 Gb density. In the future, this can be extended to over 500, or even 1,000 layers. As a result, one X-HBM die can replace all the DRAM dies used in today's HBM to significantly reduce cost and power consumption while delivering up to 16X higher bandwidth.



The X-HBM die can attach to a controller or GPU chip using hybrid bonding technology — an advanced interconnect technology with an ultra-fine 0.5μm pitch that's 10% of TSV's pitch. As a result, the data bus width can be expanded from 2,000 to 32,000 bits, delivering a 16X increase in data bandwidth.

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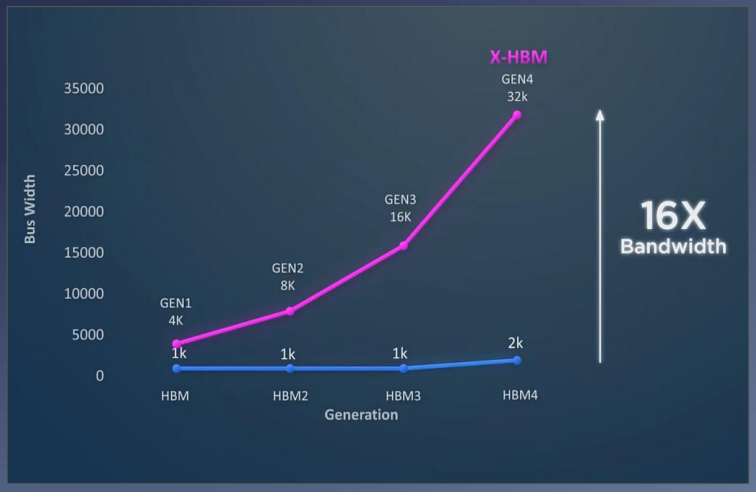
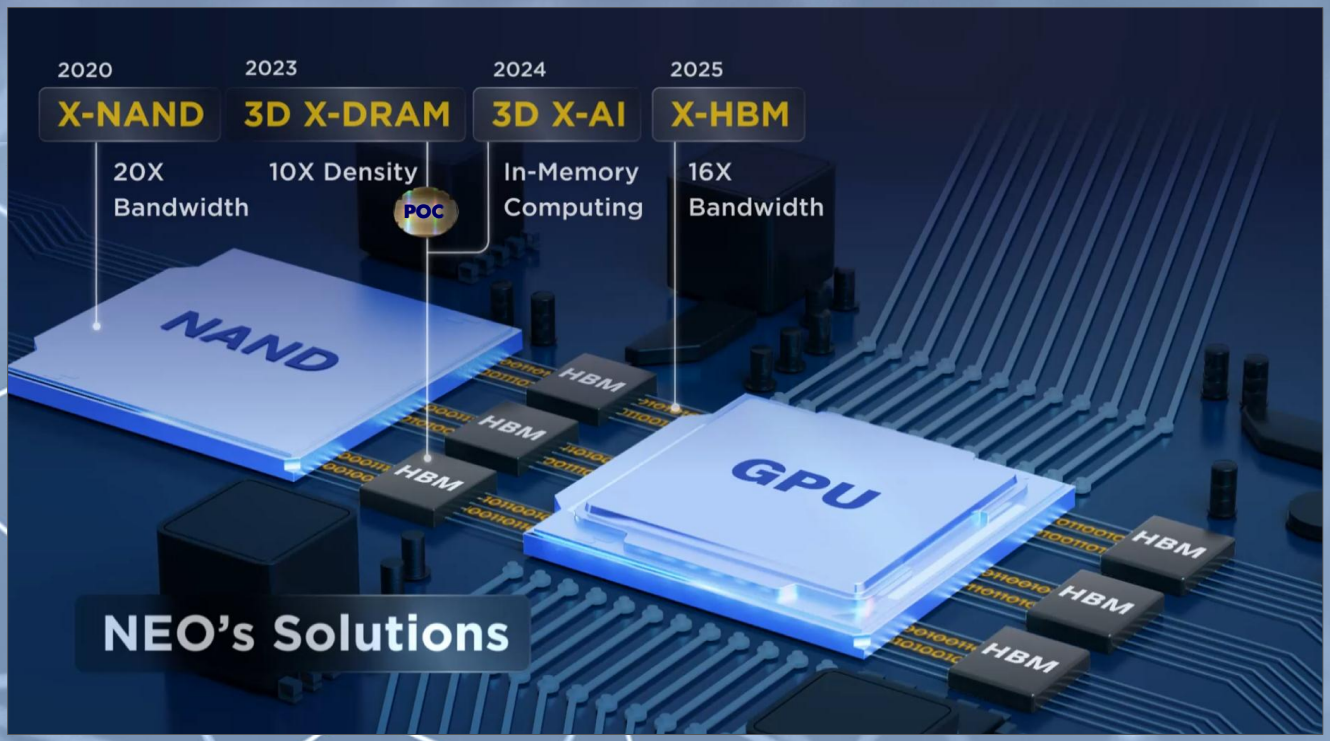


Traditional 2D DRAM increases density by shrinking cell size, with projections indicating that 2D DRAM will reach a density of up to 48 Gb at the 0a node. In contrast, 3D X-DRAM boosts density by stacking more layers. Estimates suggest it can achieve up to 512 Gb with 512 layers — offering 10 times the density of traditional 2D DRAM.

Traditional HBM, which relies on through-silicon via (TSV) technology, is expected to reach a maximum bus width of just 2,000 bits with HBM4. In contrast, X-HBM, utilizing advanced hybrid bonding, can expand the bus width by 16X to 32,000 bits — while significantly reducing power consumption and unlocking exceptional performance for AI applications.



NEO Semiconductor offers a comprehensive suite of solutions to overcome multiple memory bottlenecks limiting the full potential of AI.

- X-NAND -- brings ultra-fast read speeds to storage systems
- 3D X-DRAM -- breaks through the density limitations of traditional DRAM
- 3D X-AI -- enables AI processing inside 3D X-DRAM
- X-HBM -- delivers 16X higher bandwidth than conventional HBM